

# Five-Level Inverter Using POD PWM Technique

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**Abstract**—This paper explains the implementation of single phase 5 level inverter with Dc link Switches based on POD technique .The proposed multi level inverter is capable of generating 5 level output with less component count .This technique uses single carrier wave and two sine waves for pulse generation .The entire system is designed and implemented using MATLAB/Simulink .The inverter is connected to a R-load and performance are analyzed .Hardware is implemented using PIC16F877A micro controller.

**Keywords**—Electro Magnetic Interference (EMI); Micro controller; Multilevel-inverter; POD technique; Pulse width modulation (PWM).

## I. INTRODUCTION

Now a day's Multi level inverter are extensively used due to their increased power rating, reduced EMI , improving harmonic performance. Multi level inverters are switched at low switching frequency when compared to two level inverters, hence the switching losses are almost negligible .The multi level converter topology has drawn tremendous interest in the power industry since it can provide the high power required for high power applications.. To cope up with the problems associated with the two-level inverter, multi-level inverters (MLIs) are introduced [1]. The inverter should meet the following requirements.

- To generate a pure sinusoidal output voltage.
- Inverter output current should have low total harmonic distortion (THD).

In case of a two-level inverter, the switching frequency should be high or the inductance of the output filter inductor need to be big enough to satisfy the required THD, hence multi-level inverters (MLIs) are introduced for grid connected inverter [3-5].

Multi level inverters are classified into 3 types

- Diode clamped multi level inverter.
- Cascaded H bridge multi level inverter.
- Flying capacitor type multi level inverter

The applications of multilevel inverter are reactive power compensation, variable speed drives etc[6-8]. The topological structure of Multi level inverters should be capable of withstanding high input voltage for high power applications. A new multi level inverter is proposed which is capable of reducing problems faced by usage of conventional multi level inverters [2].

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. Furthermore, several IEEE conferences now hold entire sessions on multilevel power conversion. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation, and for high power applications.

There are many limitations in extracting power from renewable energy resources. To minimize the power demand and scarcity we have to improve the power extracting methods. Multilevel inverter is used to extract power from solar cells. It synthesizes the desired ac output waveform from several dc sources. This paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform. Harmonics Elimination was implemented to reduce the Total Harmonics Distortion (THD) value. MLI shows hope to reduce initial cost and complexity hence it is apt for industrial applications.. Simulation work is done using the MATLAB software.

The advantages of proposed multi level inverter when compared with conventional Multi level inverter are : 1. Number of devices of the proposed multi-level inverter is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.2. Only one carrier signal is required to generate switching pulses to 8 switches used in proposed Multi level inverter [1]. One of the important issues about multi-level inverter is the voltage balance of the dc-link capacitor. The voltage of capacitor C1 and C2 should be equally balanced to VDC/2.

If the capacitor voltage is unbalanced, the output voltage becomes unsymmetrical and it results in a high harmonic content in the load current.

In case of the N-level NPC type multi-level inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range +VDC to -VDC. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Three dispositions of the carrier signal to generate the PWM signal [9-11] are considered as follows;

1) Phase disposition (PD); where all carriers are in phase.

- 2) *Alternative phase opposition disposition (APOD)*; where each carrier is phase shifted by 180 degree from its adjacent carrier.
- 3) *Phase opposition disposition (POD)*; where the carriers above zero voltage are 180 degree out of phase with those below zero voltage.

## II. PROPOSED CASCADED MULTILEVEL INVERTER

Fig.1 illustrates the proposed multi level inverter which is based on cascaded H bridge multi level inverter. In the proposed multi level inverter two dc link capacitors C1 and C2 and 8 switches are used .Input supply to inverter is  $V_{dc}$  and voltage across each capacitor is  $V_{dc}/2$  . The output of the inverter is connected to LC filter in order to eliminate the harmonics . The switching sequence to generate 5 level output is shown in Fig.2.

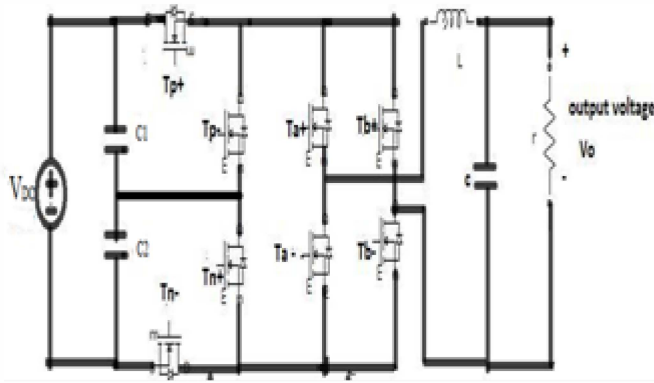


Fig. 1. Proposed five-level multi level inverter

Specifications of proposed inverter are as follows;

|                        |                  |
|------------------------|------------------|
| Input DC voltage       | :100 volts       |
| Output Voltage         | : 50 volts (rms) |
| Output Power           | : 250 watts      |
| Filter inductance (L)  | : 300 $\mu$ H    |
| Filter capacitance (C) | : 150 $\mu$ F    |

TABLE I. SWITCHING CONDITIONS OF MULTI-LEVEL INVERTER

| Output Voltage | Switching Conditions |         |         |         |         |         |         |         |
|----------------|----------------------|---------|---------|---------|---------|---------|---------|---------|
|                | $T_p^+$              | $T_p^-$ | $T_n^+$ | $T_n^-$ | $T_a^+$ | $T_b^-$ | $T_a^-$ | $T_b^+$ |
| $V_{dc}$       | ON                   | OFF     | OFF     | ON      | ON      | ON      | OFF     | OFF     |
| $V_{dc}/2$     | OFF                  | ON      | OFF     | ON      | ON      | ON      | OFF     | OFF     |
| $V_{dc}/2$     | ON                   | OFF     | ON      | OFF     | ON      | ON      | OFF     | OFF     |
| 0              | OFF                  | ON      | ON      | OFF     | ON      | ON      | OFF     | OFF     |
| 0              | OFF                  | ON      | ON      | OFF     | OFF     | OFF     | ON      | ON      |
| $-V_{dc}/2$    | OFF                  | ON      | OFF     | ON      | OFF     | OFF     | ON      | ON      |
| $-V_{dc}/2$    | ON                   | OFF     | ON      | OFF     | OFF     | OFF     | ON      | ON      |
| $-V_{dc}$      | ON                   | OFF     | OFF     | ON      | OFF     | OFF     | ON      | ON      |

## A. POD Technique for Pulse Generation

The proposed technique is based on POD technique. POD stands for phase opposition and disposition technique . The proposed technique is used for pulse generation in multi level inverter shown in figure 1 .In figure 3 if sine wave1 is greater than carrier wave ,switches  $T_p^+$  is on else  $T_p^-$  is on . If sine wave 2 is greater than carrier wave ,switch  $T_n^+$  is on else switch  $T_n^-$  is on .If sine wave 1 is positive then switches  $T_a^+$ ,  $T_b^-$  are on and if sine wave is negative then switches  $T_a^-$ ,  $T_b^+$  is on .

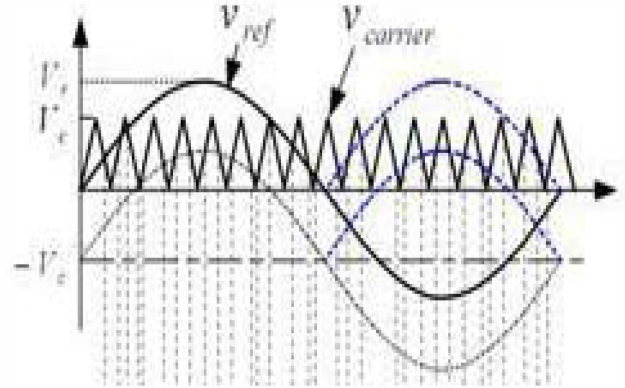


Fig. 2. Pulse generation using POD technique

## III. SIMULATION ANALYSIS AND RESULTS

Simulation of proposed multi level inverter is carried out in MATLAB/Simulink .In Figure 4 Dc supply of 100 volts is given using batteries and 2 dc link capacitors are used and 8 MOSFET are used as switches and output of multi level Inverter is connected to L,C filter to eliminate harmonics. The technique used for pulse generation is POD technique .Generally in order to turn on 8 switches 8 carrier signals are needed but using proposed technique single carrier wave is used to generate switching pulses to 8 switches. Voltage measurement device is connected across each capacitor to measure the voltage across the capacitor.

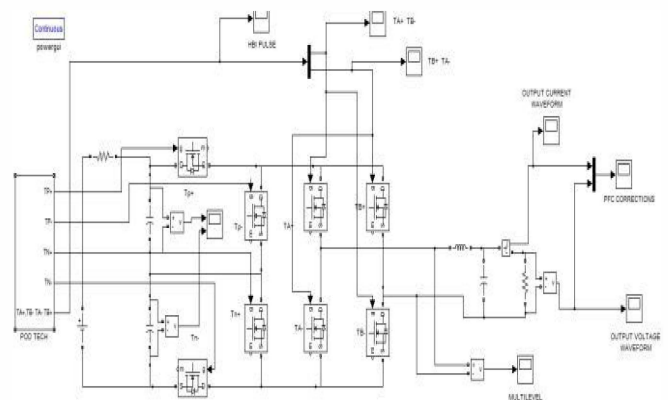


Fig. 3. SIMULINK model of proposed five-level inverter

For the simulation of five-level inverter, single carrier wave and two sine waves are generated as shown in Fig.5. Reference voltage for first sine wave is set as 1.7 volts and reference voltage for second sine wave is set as 0.8 volts. Both sine waves are operating at frequency 50 Hz. Time period for one carrier wave is set as 800 ms. In Fig.3 DC supply of 100 volts is provided as input. Voltage is divided equally across two capacitors. Voltage across each capacitor is 50 volts. Voltage across each capacitor is measured using voltage measurement device. The output of Multilevel Inverter is connected to LC filter in order to eliminate harmonics and pure sine wave is obtained. Load Voltage are measured using voltage measurement device and Load current is measured using current measurement device. This type of MLI is mainly used for grid connected applications.

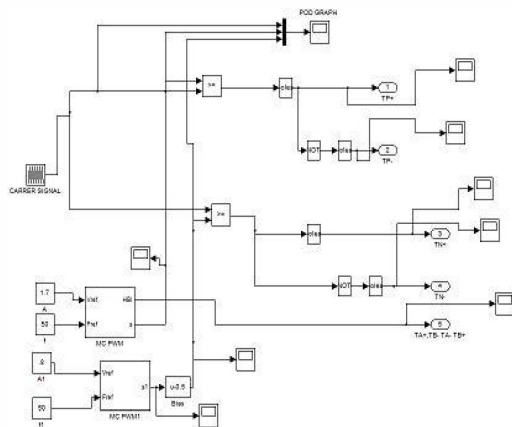


Fig. 4. SIMULINK model for switching pulse generation

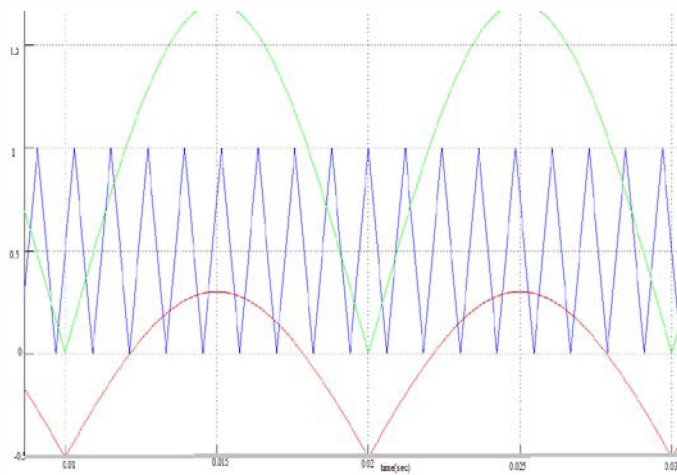


Fig. 5. Two sine reference waves and triangle carrier wave

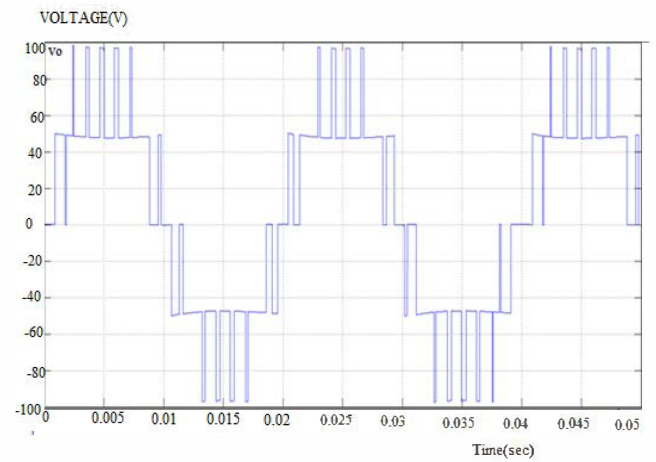


Fig. 6. Multi level inverter output voltage without LC filter

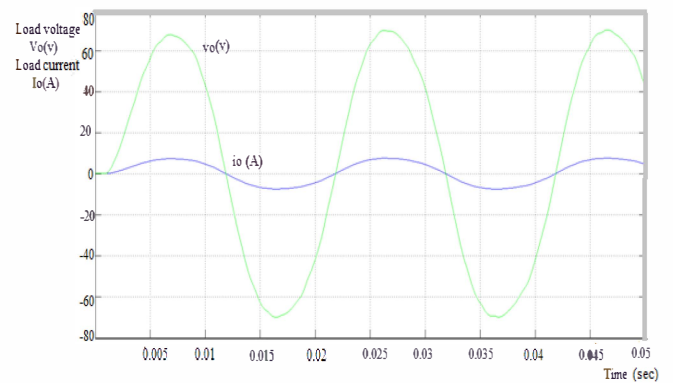


Fig. 7. Load voltage and load current (R-Load) with LC filter

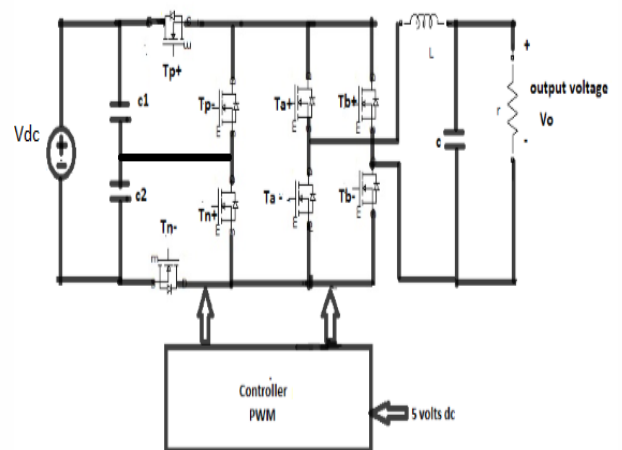


Fig. 8. Proposed single phase five-level inverter system

#### IV. EXPERIMENTATION AND RESULTS DISCUSSIONS

The major components used for experimental implementation of the proposed five-level inverter are as follows:

- PIC16F877A controller
- MOSFET IRFP460
- 6N137 opto coupler
- Pn2222a, 2n2905a transistors
- 1N4007 Diode

Fig.9 illustrates the PIC control circuit using low cost PIC16F877A microcontroller. The pulses generated from PIC circuit are amplified from 5 volts to 9 volts using Opto coupler driver IC 6N137 circuit which then fed to the switching devices of inverter. Also, Opto coupler provides isolation between control circuit and power circuit. Fig.10 describes schematic of driver circuit to amplify the voltage level of switching pluses. Fig.11 illustrates experimental prototype of proposed single phase five-level inverter.

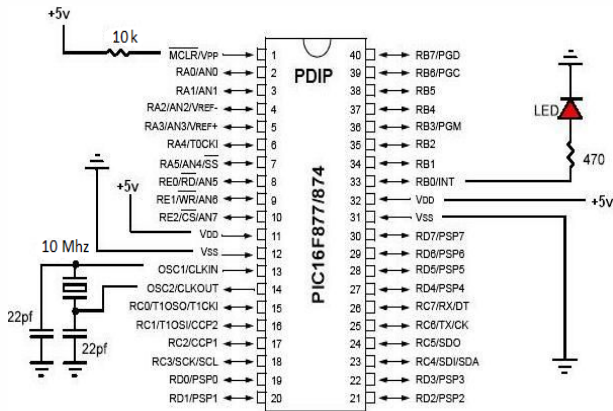


Fig. 9. Control circuit using PIC16F877A microcontroller

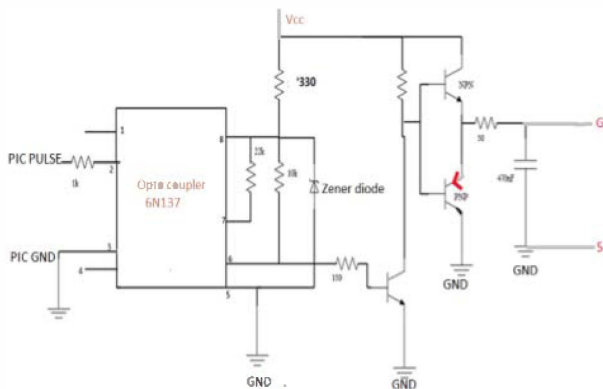


Fig. 10. Schematic of driver circuit

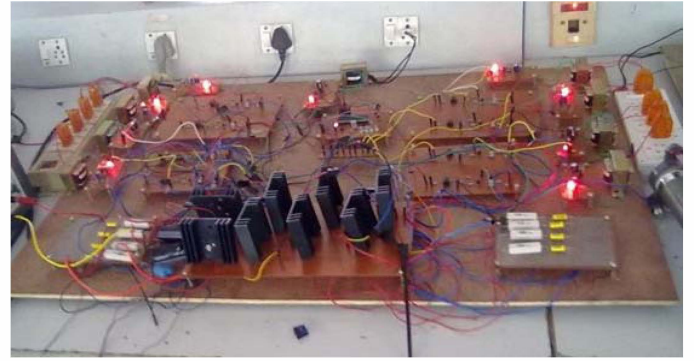


Fig. 11. Experimental setup of five-level inverter

Fig.12 depicts switching pulses of five-level inverter obtained from PIC microcontroller. Fig.13 illustrates the amplified signal of inverter switching pulse for the switch ( $T_{P+}$ ). Similarly, all other switching pulses are amplified using driver circuit which are not been shown this paper. Fig.14 depicts the output voltage waveform of proposed five-level inverter.

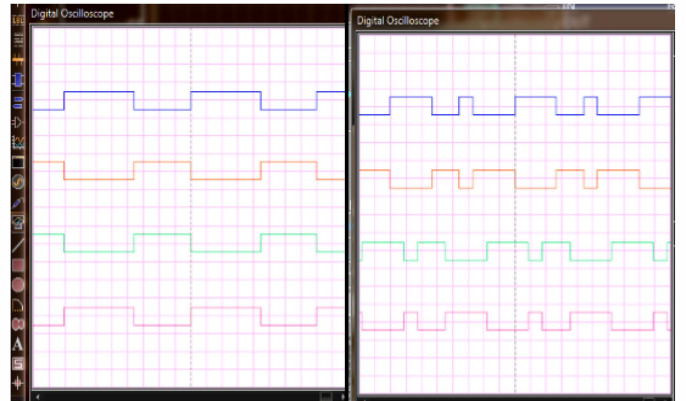


Fig. 12. switching pulses of five-level inverter obtained from PIC microcontroller

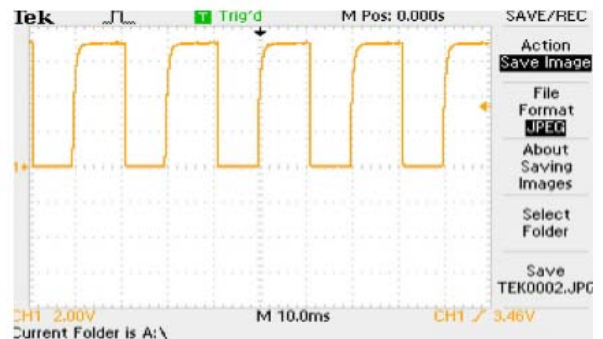


Fig. 13. Inverter Switching pulse for the switch ( $TP+$ )

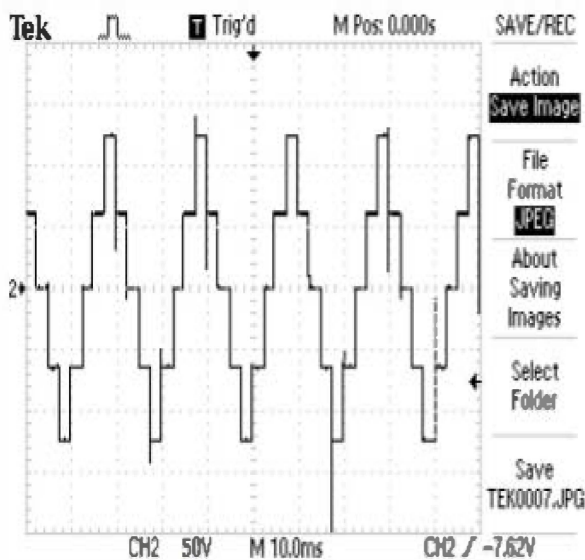


Fig. 14. Output voltage waveform of five-level inverter

## V. CONCLUSION

A new Five level inverter topology using POD technique is designed and the same is implemented in MATLAB/Simulink which is capable of producing 5 level output with less component count. No of dc supply sources used in proposed multi level inverter are less when compared to conventional Cascaded H bridge multi level inverter. The proposed MLI has the following advantages over the conventional inverters:

- Proposed topology can be easily extended to 9-level or higher level with minimized active device component count
- Switches are turned on at low switching frequency (50Hz). Hence switching losses are almost negligible.
- Single H bridge is used to produce 5 level output
- No of DC link capacitors used to produce 5 level output is less when compared to conventional cascaded H-bridge multilevel inverter

## Acknowledgment

We sincerely express and acknowledge resourceful valuable guidance and financial support given by Center of Excellence under TEQIP, national Institute of Technology Warangal for providing necessary facilities. I also want to

thank my guide Dr Narsimharaju B. L, Faculty of Electrical Engineering, Prof. Srinivasa Rao.S Faculty of Mechanical Engineering who had encouraged me to write this paper.

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